IN THE SPECIFICATION

Please delete the heading and paragraphs beginning at page 5, line 11 to page 6, line 15, and insert the following replacement heading and paragraphs, as follows:

Exemplary Embodiments for Solving the Problem

In a first exemplary embodiment of the present invention, a data processor is provided, the data processor comprising:

a CPU configured to control an entire system;

a DSP configured to perform preset processing, to have at least two bus cycles in a unit of one data access, and to use a selectable number of the bus cycles in the unit of one data access; and

an external memory configured to be accessed by the DSP and to be accessed through the DSP by the CPU, wherein

a data word length accessed by the DSP at the external memory is variable, and

the DSP includes

a determination unit configured to determine whether the DSP is accessing the external memory;

a control unit configured to determine whether the CPU is allowed to access the external memory, based on a signal from the determination unit; and

a switching unit configured to perform a switching operation of an address and a data in connection with the external memory according to a command from the control unit, and to input and to output the address and the data based on the switching operation,

wherein when the DSP accesses the external memory using a maximum number of the bus cycles in a unit of data access wherein the DSP actually accesses the external memory, access from the CPU to the external memory is placed in a wait state until a subsequent unit of data access commences, and

when the DSP does not access the external memory using the maximum number of the bus cycles in said unit of data access wherein the DSP actually accesses the external memory, access from the CPU to the external memory is constantly allowed during said unit of data access.

Please amend the paragraph beginning at page 6, line 16 to page 7, line 11, as follows:

In accordance with the above-mentioned structure, in a case where the data word length is selected so as to perform accessing by a maximum number (e.g., such as three bus cycles) of the bus cycles (e.g., one word = 24-bit mode), when the determination ~~means~~ unit determines that the DSP is accessing the external memory, the access from the CPU to the external memory is placed in a wait state by the control ~~means~~ unit, and in a case where the data word length is not selected so as to perform accessing by a maximum number of the bus cycles (e.g., one word = 16-bit mode), the control ~~means~~ unit allows the CPU to access the external memory by utilizing a free bus cycle. Accordingly, when there is a free bus cycle, the bus cycles are fixed (in other words, a free bus cycle in, e.g., a 16-bit mode is fixed for access from the CPU so that the CPU is allowed to access the external memory at the free bus cycle), and, when there is no free bus cycle, the operation is switched to a method wherein access from the DSP takes precedence (in other words, when there is no free bus cycle as in, e.g., the 24-bit mode, the bus cycles are basically used for access from the DSP, and only when there is no access from the DSP, the CPU is allowed to access the external memory).

Please delete the paragraphs beginning at page 7, line 12 to page 9, line 19 and insert the following replacement paragraphs, as follows:

In a second exemplary embodiment of the present invention, a data processor is provided, the data processor comprising:

a CPU configured to control an entire system;

a sound source configured to supply a musical tone signal;

a DSP configured to perform preset processing to apply a desired effect to the musical tone signal supplied from the sound source, to have at least two bus cycles in a unit of one data access with respect to signal processing of the musical tone signal, and to use a selectable number of bus cycles in the unit of one data access; and

an external memory configured to be accessed by the DSP and to be accessed through the DSP by the CPU, wherein

a data word length accessed by the DSP at the external memory is variable, and

the DSP includes

a determination unit configured to determine whether the DSP is accessing the external memory;

a control unit configured to determine whether the CPU is allowed to access the external memory, based on a signal from the determination unit; and

a switching unit configured to perform a switching operation of an address and a data in connection with the external memory according to a command from the control unit, and to input and to output the address and the data based on the switching operation,

wherein when the DSP accesses the external memory using a maximum number of the bus cycles in a unit of data access wherein the DSP actually accesses the external memory, access from the CPU to the external memory is placed in a wait state until a subsequent unit of data access commences, and

when the DSP does not access the external memory using the maximum number of the bus cycles in said unit of data access wherein the DSP actually accesses the external memory, access from the CPU to the external memory is constantly allowed during said unit of data access.

Further, a third exemplary embodiment of the present invention includes a data processor having a fixed number of memory access timings per sampling cycle. The data processor comprises:

a plurality of DSPs configured to access a single external memory in a single package;

a read/write control unit configured so that when each of the DSPs issues a read command or a write command at a same time, none of the commands from the DSPs are performed and when only one of the DSPs issues the read command or the write command, the command from the only one DSP is performed;

an access determination unit configured so that when each of the DSPs issues the read command or the write command at the same time, none of the DSPs are not allowed to access the external memory and when the only one of the DSPs issues the read command or the write command, the only one DSP is allowed to access the external memory;

a first selector configured to output an address from the allowed DSP in response to a determination signal from the access determination unit; and

a second selector configured to output data from the allowed DSP in response to the determination signal, wherein

each of the DSPs includes a control unit configured to acquire data from the external memory in response to the determination signal from the access determination unit, and

the read/write control unit does not access the external memory when each of the DSPs simultaneously issues a command.

Please amend the paragraph beginning at page 9, line 20 to page 10, line 14, as follows:

In accordance with the ~~above-mentioned~~ structure of the third exemplary embodiment, when each of the DSPs issues a read command or a write command at the same timing, the read/write control ~~means~~ unit controls the command of which DSP is allowed, and when each of the DSPs issues a read command or a write command at the same timing, the access determination ~~means~~ unit determines which DSP is allowed to perform memory access. The first selector outputs an address from the allowed DSP in response to a determination signal from the access determination ~~means~~ unit, and the second selector outputs a data from the allowed DSP in response to the determination signal. On the other hand, a DSP, which is allowed to perform memory access to read out a data by the access determination ~~means~~ unit, acquires, from the control ~~means~~ unit for data acquisition, such a data output from the external memory in response to the determination signal from the access determination ~~means~~ unit, the control ~~means~~ unit for data acquisition being included in the allowed DSP. These ~~means~~ units are combined, providing the data processor wherein the plural DSPs are formed in one package, and the DSPs can share the single external memory.

Please delete the paragraphs beginning at page 10, line 15 to page 11, line 10 and insert the following replacement paragraphs as follows:

In a fourth exemplary embodiment of the present invention, a data processor having a fixed number of memory access timings per sampling cycle is provided, the data processor comprising:

a plurality of DSPs configured to access a single external memory in a single package, the external memory storing musical tone waveform data;

a read/write control unit configured so that when each of the DSPs issues a read command or a write command at a same time, none of the commands from the DSPs are performed and when only one of the DSPs issues the read command or the write command, the command from the only one DSPs is performed;

an access determination unit configured so that when each of the DSPs issues the read command or the write command at the same time, none of the DSPs are not allowed to access the external memory and when only one of the DSPs issues the read command or the write command, the only one DSP is allowed to access the external memory;

a first selector configured to output an address from the allowed DSP in response to a determination signal from the access determination unit; and

a second selector configured to output data from the allowed DSP in response to the determination signal, wherein

each of the DSPs includes a control unit configured to acquire data from the external memory in response to the determination signal from the access determination unit, and

the read/write control unit does not access the external memory when each of the DSPs simultaneously issues a command.

Please amend the paragraph at page 11, lines 11-25, as follows:

When musical tone waveform data are output form plural channels, two or more DSPs, which apply an effect to a musical tone waveform data, are used, depending on the number of the effects to be applied (including a case where different kinds of effects are applied), in some cases. It is considered to be reasonable in terms of a reduction in power consumption and improvement in processing speed that the provision of plural DSPs, which is caused by an increase in signal processing using DSPs, is realized as one package to form a system LSI. In the fourth exemplary embodiment ~~As defined in Claim 5~~, a data processor,

wherein plural DSPs are put into one package, and these DSPs can share a single external memory, is proposed to be used as a structure for applying an effect to a musical tone waveform data.

Please amend the paragraph beginning at page 11, line 26 to page 12, line 3, as follows:

With respect to the structures defined in the third and fourth exemplary embodiments ~~Claim 3 and 5~~, it is preferred that the read/write control ~~means~~ unit be controlled so as not to access the external memory when the respective DSPs issue plural commands ~~(see Claims 4 and 6)~~.

Please amend the heading and paragraph at page 12, lines 5-13, as follows:

Effect of Exemplary Embodiments of the Invention

In accordance with the data processors defined in ~~Claims 1 and 2 in connection with~~ the first and second exemplary embodiments of the present invention, the CPU is allowed to access the external memory in an interval between data accesses from the DSP having a variable data length in access. Accordingly, it is possible to have a beneficial effect of allowing the CPU to be operated so as to maximize the number of access without disturbing the access from the DSP.

Please amend the paragraph at page 12, lines 14-21, as follows:

In accordance with the data processors defined in ~~Claims 3 to 6 in connection with~~ the third and fourth exemplary embodiments of the present invention, it is possible to have beneficial effects of eliminating waste in the capacity of the external memory by providing an LSI wherein the plural DSPs are formed in one package with the DSPs being capable of

sharing a single external memory, and of making it simpler to design a circuit using the plural DSPs to perform signal processing.

Please amend the paragraph beginning at page 12, line 22 to page 13, line 3, as follows:

In particular, when two or more of DSPs are required to apply two kinds or more of effects to the waveform data of a musical tone as defined in the fourth exemplary embodiment ~~Claims 5 and 6~~, it is possible to have advantages of eliminating waste in the capacity of the external memory and of shortening the fabrication process since the peripheral parts of a circuit using the above-mentioned structure, such as an electronic musical instrument, are prevented from being complicated.